The DØ Silicon Detector for Run IIb

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For the DØ Collaboration

Outline

- Physics motivation
- Detector design
  - Design considerations
  - Design Overview
  - Expected Performance
- Project status – design and prototyping
  - Support structures
  - Readout modules
  - Sensors, readout chips, hybrids
- Summary and conclusions

Physics goals drive the upgrade

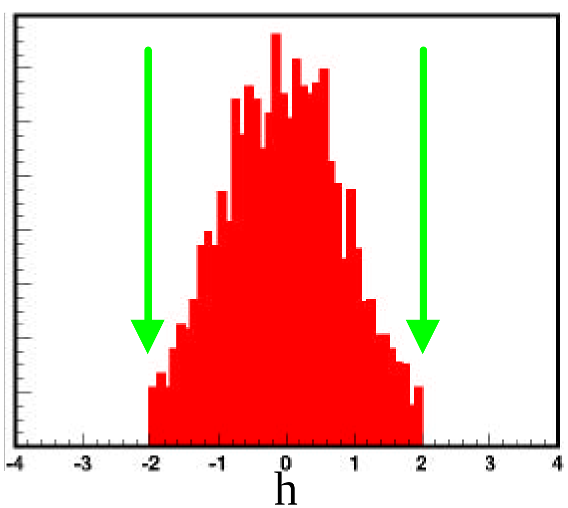
- The Director has set the goal of achieving ~15 fb^{-1} before the LHC starts producing physics

15 fb^{-1} before LHC → Integrated Luminosity → Radiation damage: Replace silicon

15 fb^{-1} before LHC → Instantaneous Luminosity → Occupancy, pattern recognition: Trigger upgrades

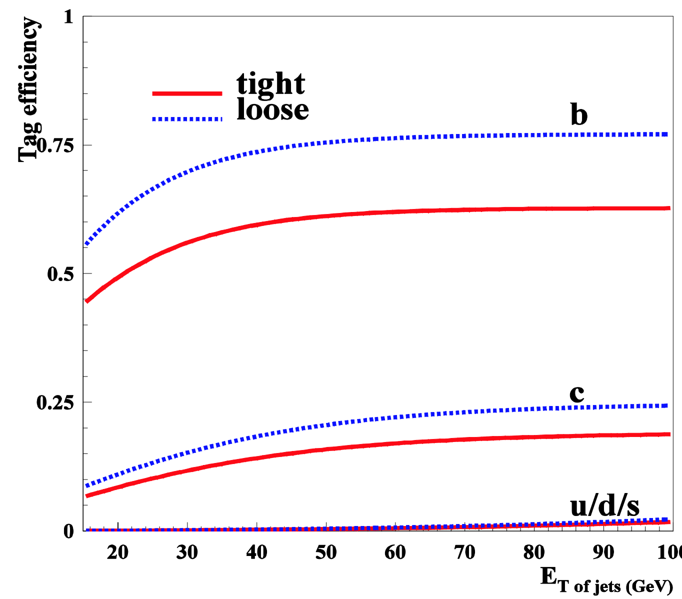
- The run IIb physics goals require efficient triggering and reconstruction of
  - isolated leptons
    - (including taus if possible)
  - jets
  - missing E_T
  - b-tagging
- Kinematic range for all objects is typically p_T > 15 GeV, $|h|$ < 2

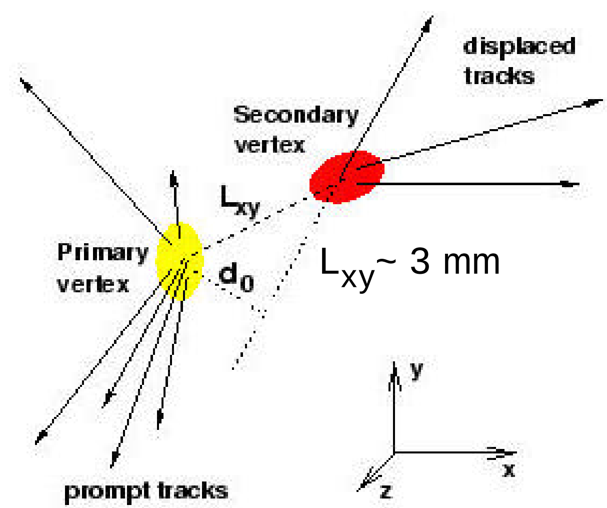
SUSY trileptons



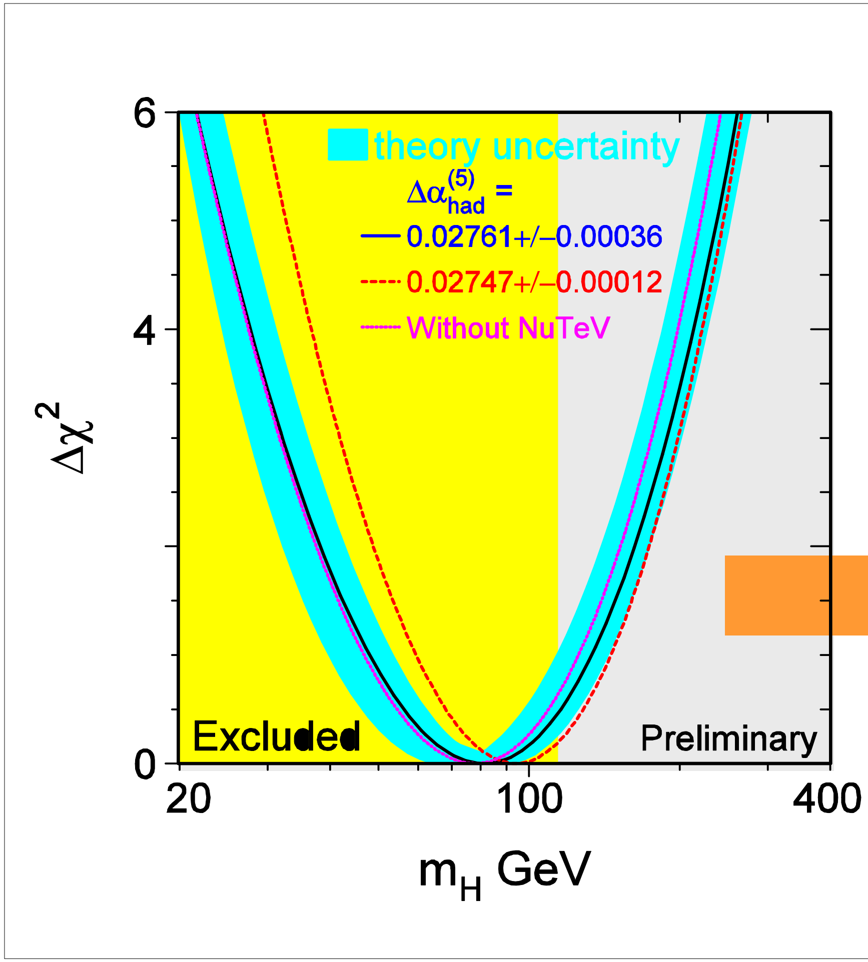
Run IIb: Higgs Potential I

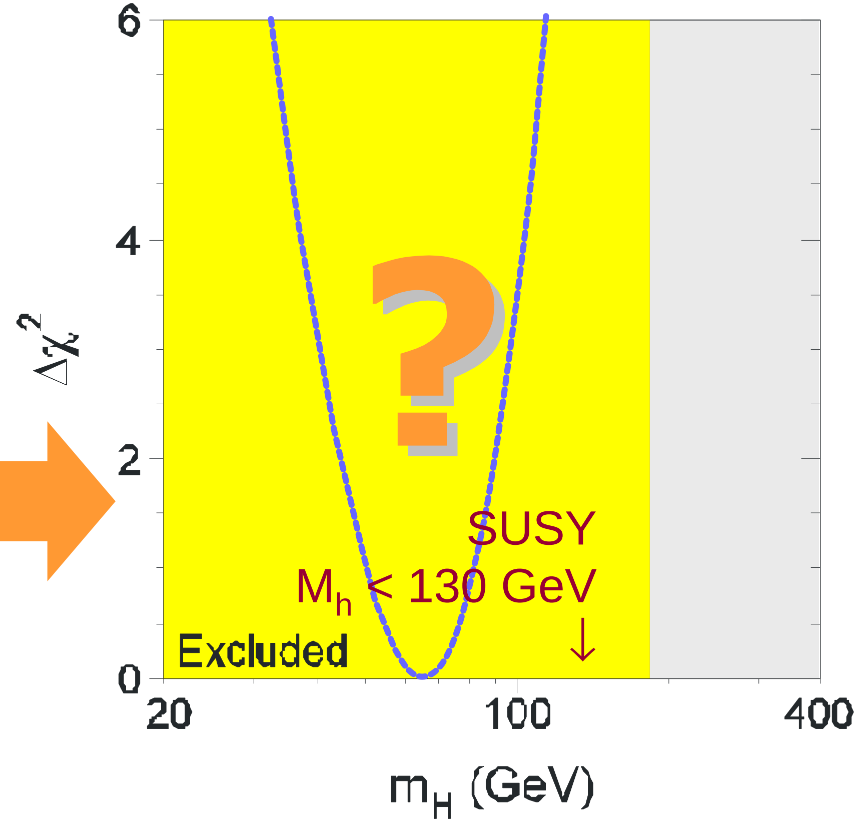
- **Higgs potential:**
  - Luminosity of 8 fb^{-1}
    - 3s discovery for m_H < 122 GeV
    - exclusion at 95% CL for m_H < 135 GeV or 150 < m_H < 180 GeV
  - Luminosity of 15 fb^{-1}
    - 5s discovery for m_H < 115 GeV
    - exclusion at 95% CL for m_H < 185 GeV
- **Assumptions of Working Group:**
  - Loose b-tag: e_b ~ 75% per jet
  - Tight b-tag: e_b ~ 60% per jet
- **Implications for current Detector**
  - Need a replacement Silicon Tracker with
  - b-tagging efficiency exceeding ~65% per jet at mistag rate < 1%
  - Radiation hard to at least ~15 fb^{-1}





Run IIb: Higgs Potential II





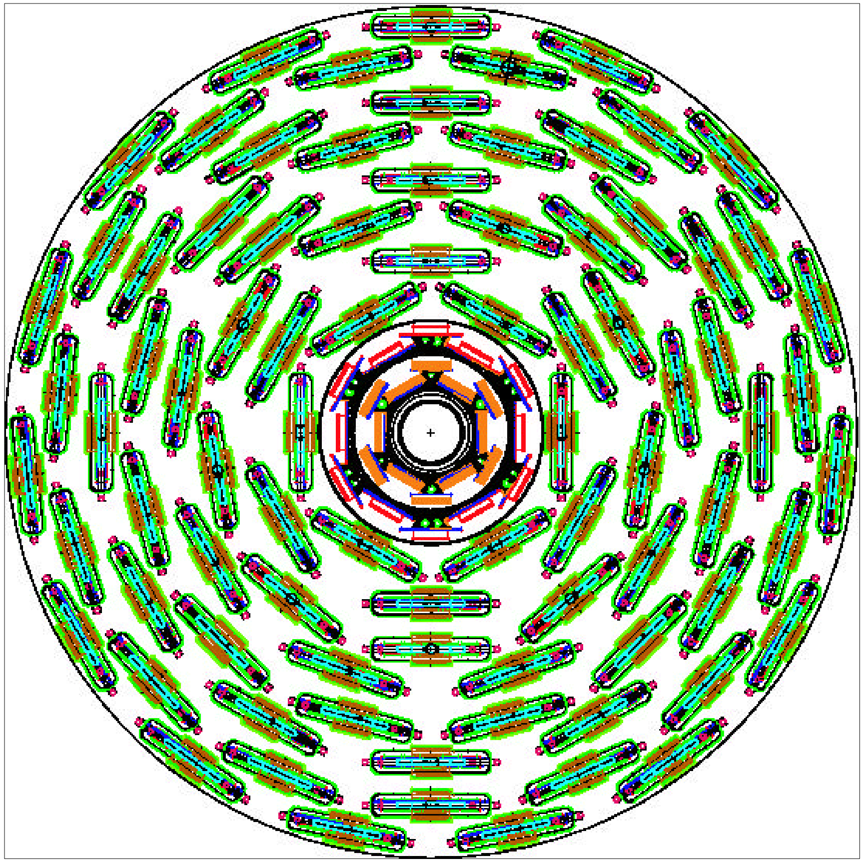
Grünewald, Heintz, Narain, Schmitt, hep-ph/0111217
Assumes current central values
$\delta\Delta\alpha^{(5)}_{had}(M_Z^2) = 10^{-4}$, $\delta M_W = 20$ MeV, $\delta m_t = 1$ GeV

Design Considerations

- **Guiding Principles**
  - Design *must* allow for expeditious assembly to be ready in 3 years
  - Minimal shutdown time to allow for accumulation of luminosity before LHC
  - Tight cost control to ensure feasibility of funding the project
- **Needed improvements over Run IIa detector**
  - Add innermost layer at smaller radius (2cm) for better vertex resolution
  - Add outermost layer, fine pitch, larger radius for pattern recognition
- **Benefit from Run IIa experience**
  - Choose design adequate to achieve physics goals, but do not over-design
  - Modular design, minimize the number of different elements
  - Use established technologies, e.g.single sided silicon only
- **Spatial constraints**
  - Installation within existing fiber tracker Þ Si outer radius of 180 mm
  - Full tracking coverage
    - In concert with fiber tracker up to $|h| < 1.6$
    - Silicon stand-alone up to $|h| < 2.0$
- **Data Acquisition and Silicon Track Trigger**
  - Retain readout system outside of calorimeter
  - Total number of readout modules cannot exceed 912
  - Respect 6-fold azimuthal symmetry

Detector Design Overview

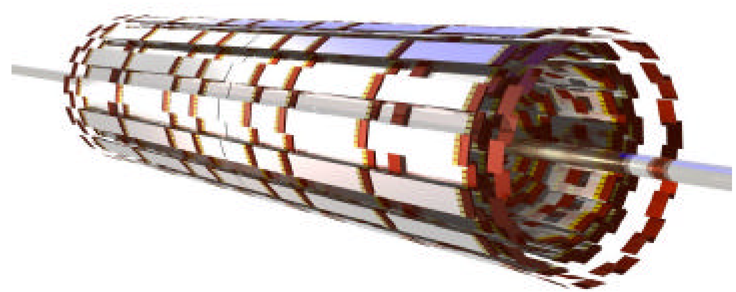
- **Six layer silicon tracker, divided in two radial groups**
  - **Inner layers: Layers 0 and 1**
    - **18mm < R < 39mm**
    - **Axial readout only**
    - **50/58 μm readout for L0/L1**
    - **Assembled into one unit**
    - **Mounted on integrated support**
  - **Outer layers: Layers 2-5**
    - **53mm < R < 164 mm**
    - **Axial and stereo readout**
    - **60 μm readout**
    - **Stave support structure**
  - **All sensors have intermediate strips**

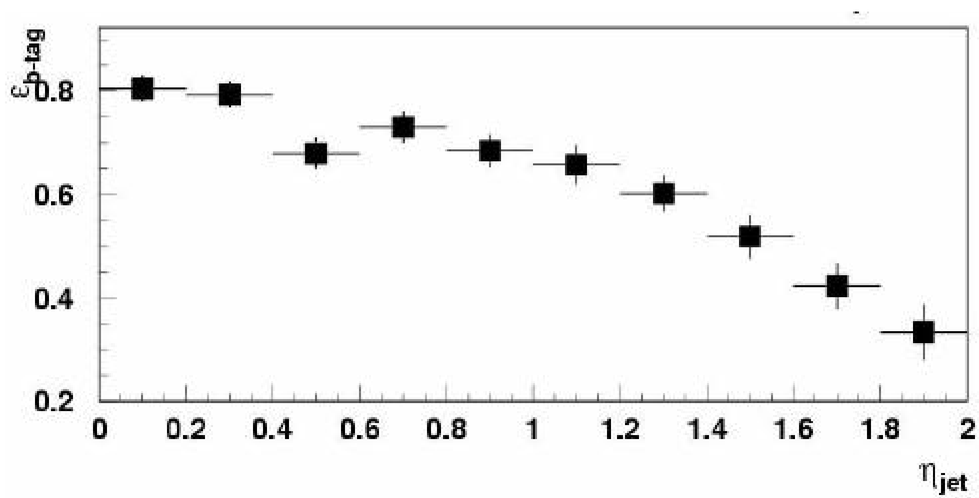


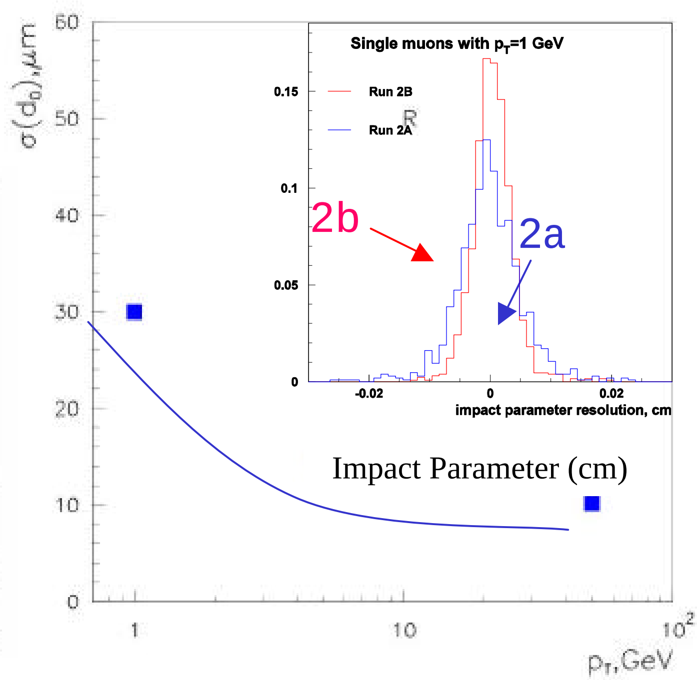
- **Employ single sided silicon only, 3 sensor types**
  - **2-chip wide for Layer 0**
  - **3-chip wide for Layer 1**
  - **5-chip wide for Layers 2-5**
- **Beampipe inserted through silicon *in situ*, supported from fiber tracker**

Performance of Proposed Detector

- **Performance studies based on full Geant simulation**
  - Full model of geometry and material
  - Model noise, mean of 2.1 ADC counts
  - Single hit resolution of ~11 μm
  - Pattern recognition and track reconstruction
- **Benchmarks**
  - $\sigma(p_T)/P_T$ ~ 3% at 10 GeV/c
  - $\sigma(d_0)^2 = 5.2^2 + (25/p_T)^2$
    - $\sigma(d_0) < 15$ μm for $p_T > 10$ GeV/c
- **b-jet tagging**
  - efficiency of ~ 65% per jet (WH events)

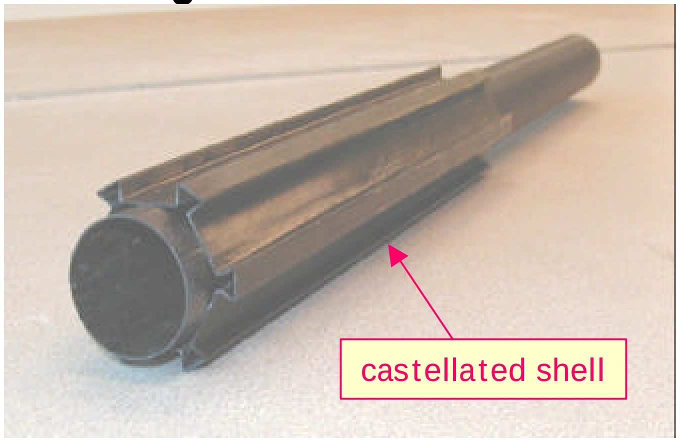




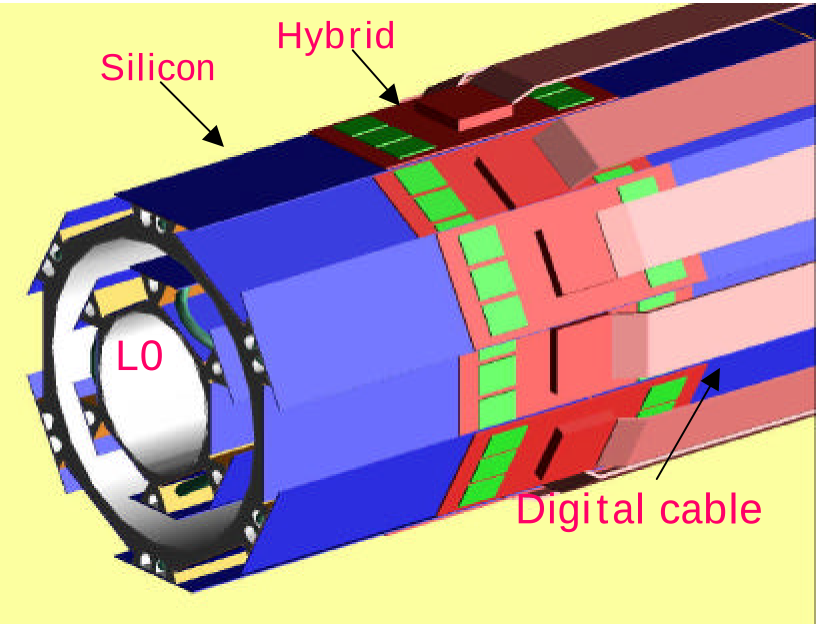


Layer 0 and 1 Supports

- **Support structure for L0 and L1 by U. of Washington**
- **Layer 0**
  - **Readout electronics outboard**
    - **Space constraints force electronics outboard**
    - **Independent cooling of sensors and hybrids**
    - **Reduced mass for better vertex resolution**
  - **Heat load of < 0.3 W/sensor after 15 fb^{-1}**
  - **To control depletion voltage rise from radiation damage, T_{Si} ~ -10 ^{0}C**

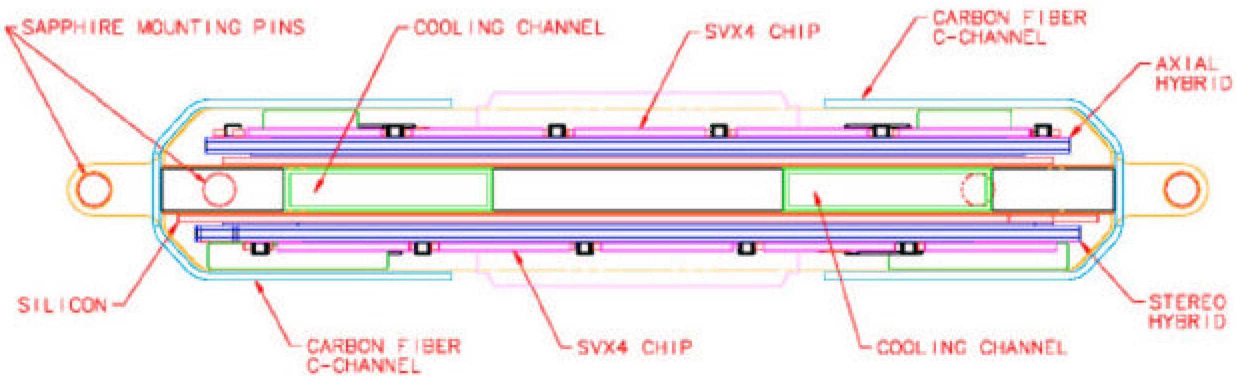


- **Layer 1**
  - **Readout electronics mounted on the sensors in L1**
  - **Power dissipation of 3W/hybrid**
    - **0.5W per SVX is conservative**
  - **Sensor power negligible**
  - **To control noise from radiation damage, T_{Si} < -5 ^{0}C**



Layer 2-5 Staves

- **Basic building block of the outer layers is a stave**

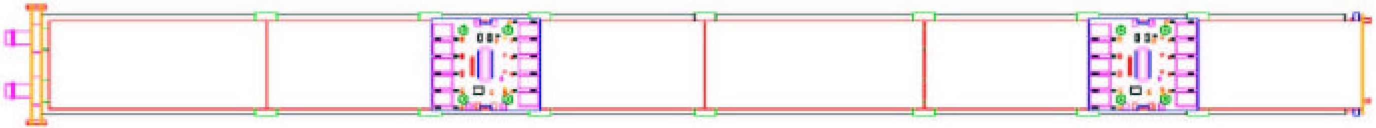


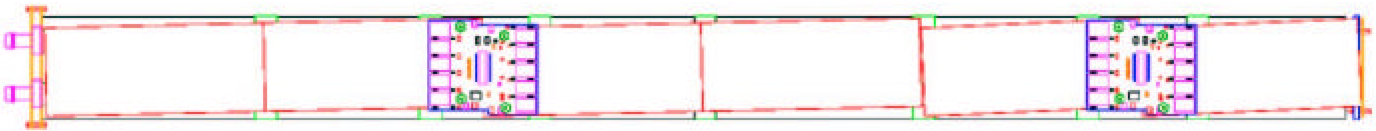
VIEW LOOKING AT Z=600 END

- **Stave design**
  - **One layer of axial readout and one layer of stereo readout**
    - **Stereo angle (1.24° or 2.48°) obtained by rotating sensors**
  - **Layers separated by a "core" with integrated cooling**
    - **Core contains positioning and reference pins**
    - **Core provides stiffness to flatten sensors**
  - **C-channels at edges of stave provide bending stiffness**
  - **Supported by carbon fiber bulkheads at z = 0 & z = 605 mm**
  - **Total of 168 staves required to populate L2-5**

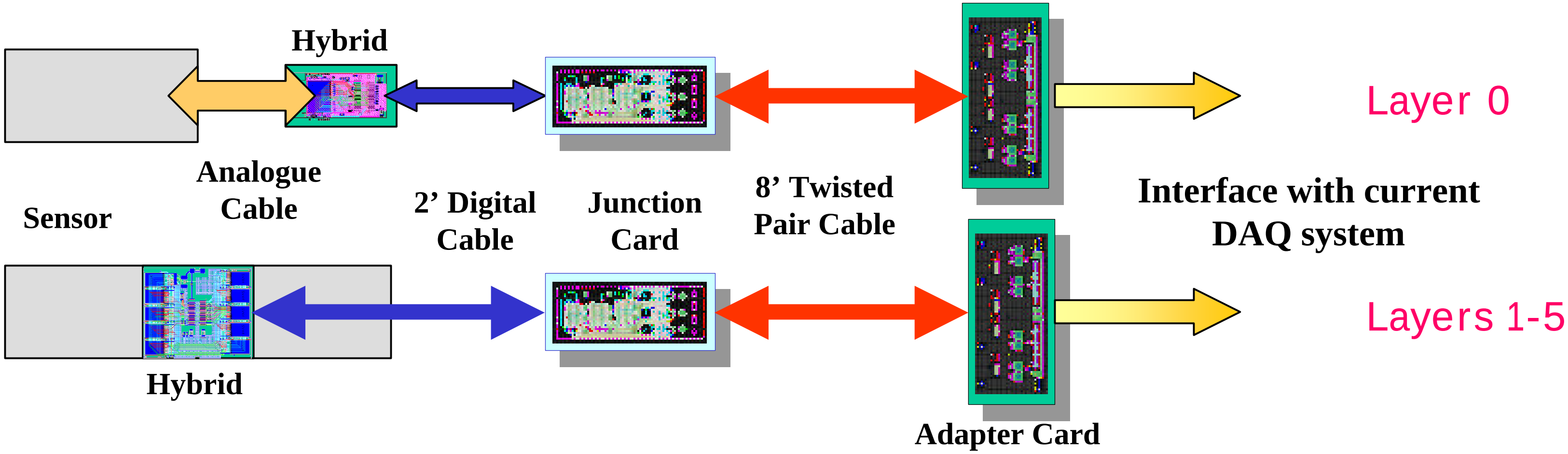
Readout Modules

- **Each stave has four readout modules**
- **Readout module lengths vary with layer and z-position.**
  - For all layers, the modules closest to z = 0 are 200 mm long
  - Those furthest from z = 0 are 400 mm long
- **Four Readout module types**
  - 10-10 (axial, stereo)
  - 20-20 (axial, stereo)
  - Ganged sensors will have traces aligned (sensors are 10cm long)
- **Each readout module serviced by double-ended hybrid**
  - Each hybrid has two independent readout segments





Readout Schematics



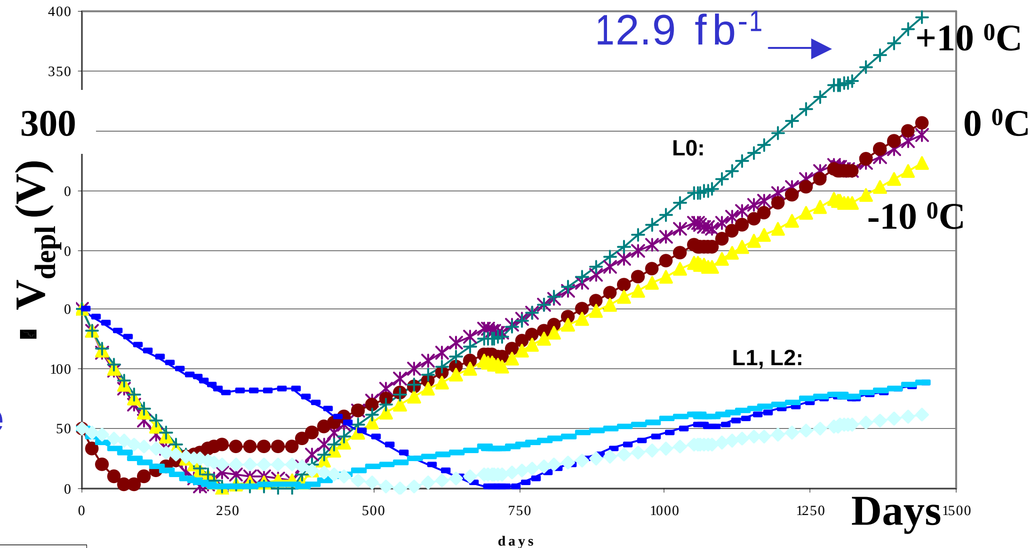
- **Layers 1-5: Hybrids mounted on silicon**
  - Hybrid -> digital cable -> junction card -> twisted pair -> Adapter Card
- **Layer 0: Hybrids mounted off-board**
  - Analogue Cable -> Hybrid -> digital cable -> junction card -> twisted pair -> Adapter Card
- **Readout with SVX4 chips operated in SVX2 mode**

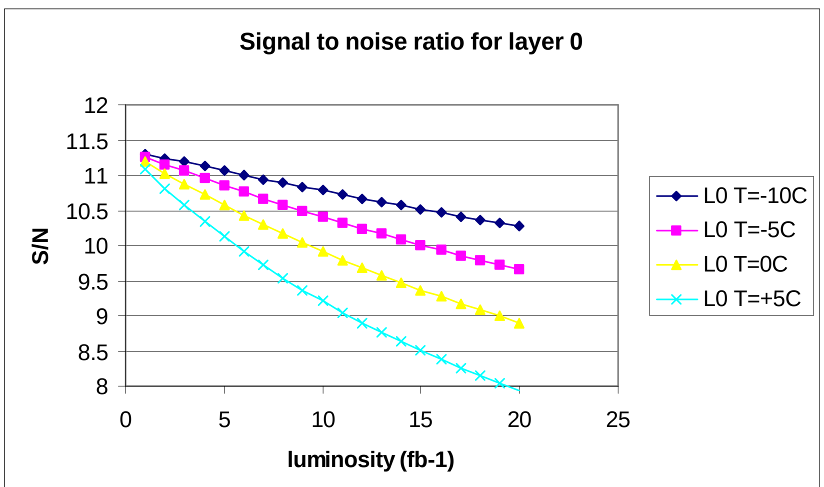
Sensors

- All sensors are single-sided silicon with axial strips only
- Layer 0
  - 2-chip wide, 50μm pitch, intermediate strips, 79.4mm cut length
  - Sensors specifications identical to CDF layer00 (Run IIa) sensors
    - HPK
      - Proven track record; manufactured CDF sensors, V_{break} > 700V, irradiated by DØ
      - ‘Old’ CDF Layer00 sensors meet all our specifications
    - ELMA
      - 60 Lyr 0 sensors produced 47 received: 20 mechanical, 27 currently being tested
- Layer 1
  - 3-chip wide, 58μm pitch, intermediate strips, 79.4mm cut length
  - Same basic design and specifications as L0
    - Prototypes received from HPK
- Layers 2-5
  - 5-chip wide, 60μm pitch, intermediate strips, 41.1x100 mm cut dimension
  - Order for prototypes placed with HPK
  - Sensors very similar to CDF outer layer sensors

Radiation Damage Requirements

- **Sensors will be subjected to fluence of 2 10^{14} 1 MeV neutron equiv./cm^2**
- **Parameters for detector**
  - V_{depl} after irradiation
  - Signal to Noise ratio
- **Requirements**
  - S/N ratio > 10 after 15 fb^{-1}
  - V_{depl} « V_{break} to allow for over-depletion for full charge collection

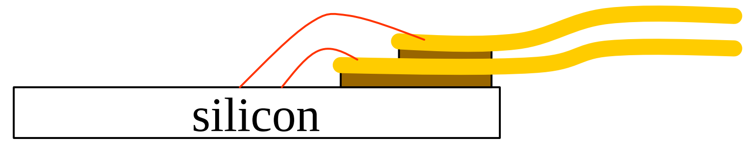


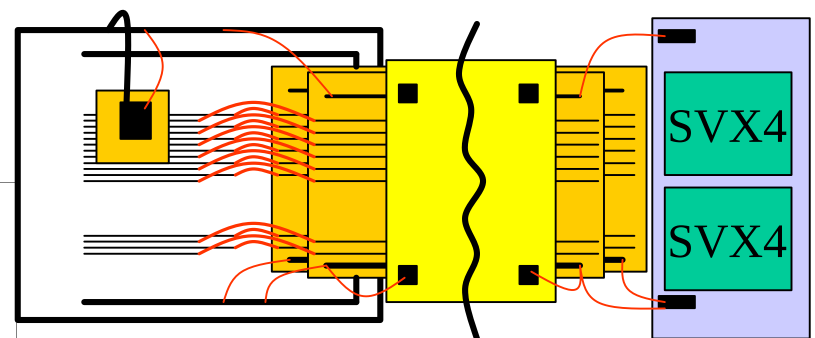


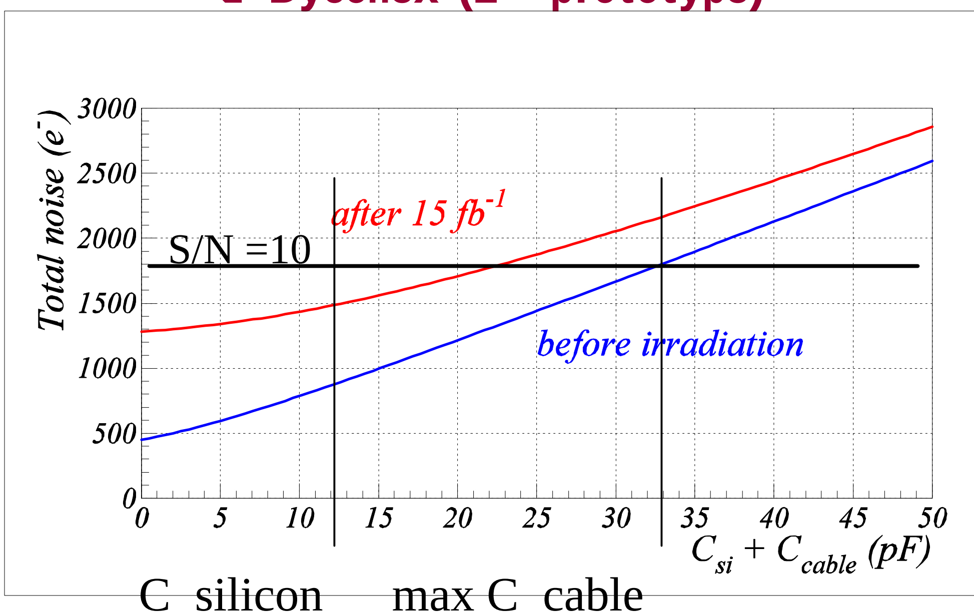
Layer	T_silicon (C)
Layer 0	-10
Layer 1	-5
Layer 2	0
Layer 3	>0
Layer 4	>0
Layer 5	>0

Analogue Flex Cables

- **For layer 0 need low mass, fine pitch flex cables to carry analogue signals to hybrids**
  - **Technically challenging**
    - **Trace width ~ 15 - 20 mm, pitch 91 mm**
    - **2 cables offset by 45 mm**
  - **Noise determined by capacitance**
    - **C < 0.55 pF/cm**
    - **Dyconex (2[nd] prototype)**



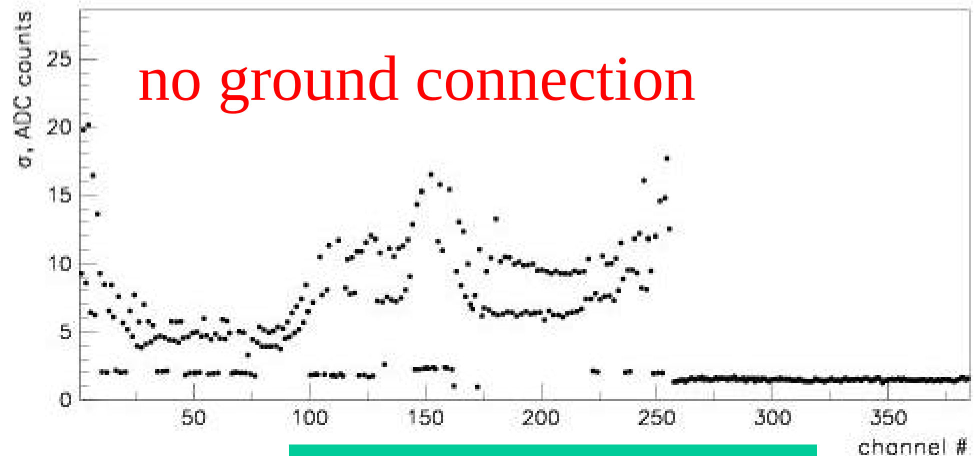




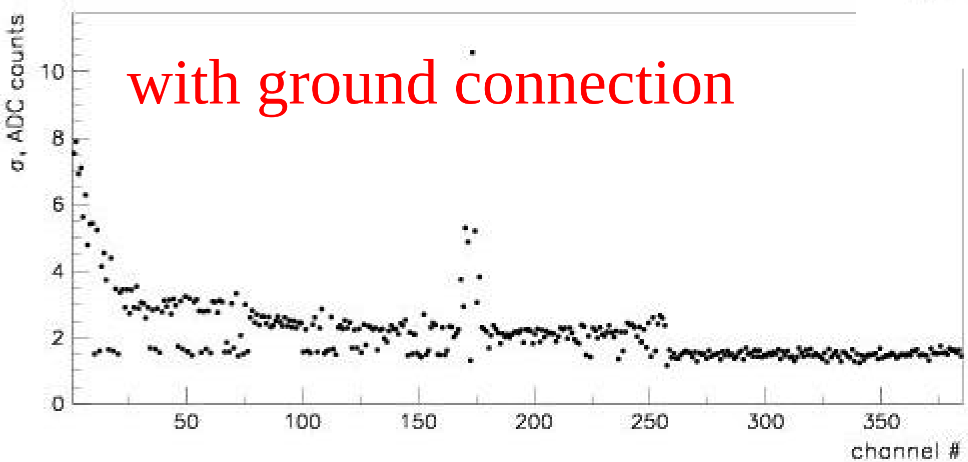
Based on FEA analysis:
16μm trace width -> 0.32 pF/cm

Analogue Flex Cable Tests

- **Second prototype cables (Dyconex, Zürich)**
  - First batch: 12 cables. Two had 2 open/shorts, remaining were good
  - Second batch: 27 cables; 16 perfect, 9 had 1 open, 2 = 2 open/short
- **Built full Layer 0 module, with Run IIa hybrid readout, 2 chips connected**
- **Study of cable shielding**
  - CDF has noise issues in L00
  - Cables run over CF structure
  - Need to eliminate pickup

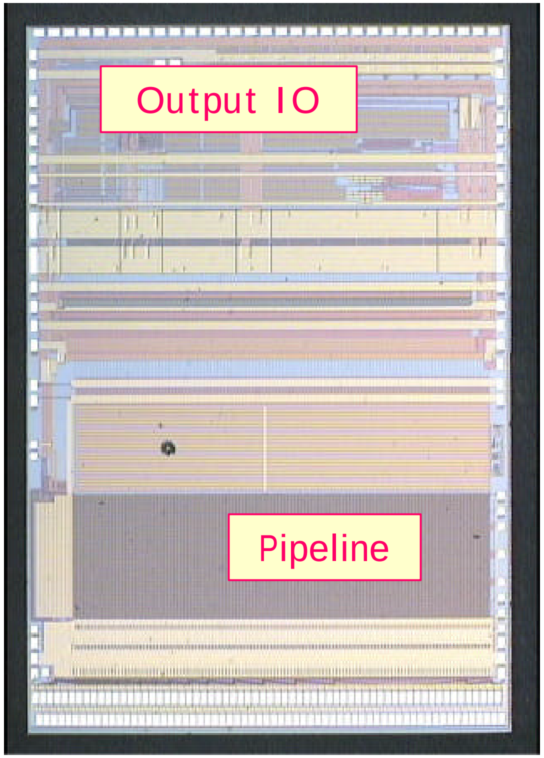


Ungrounded metal under cable



SVX4 Chip

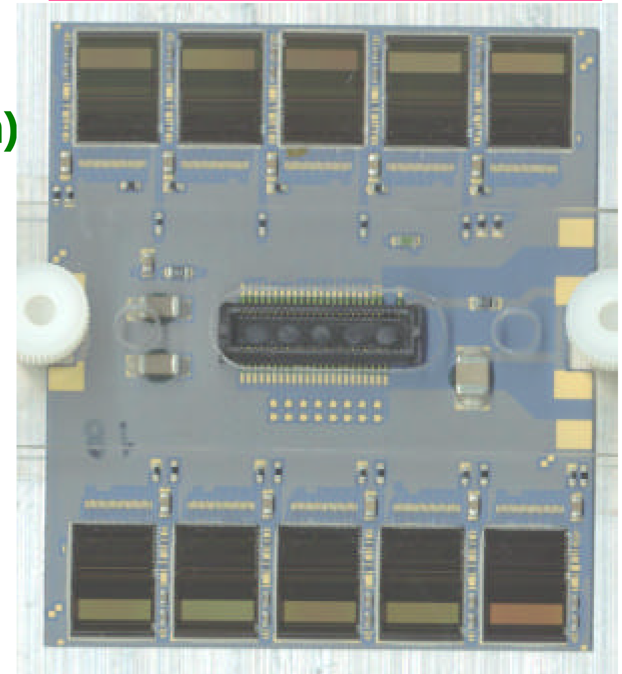
- SVX4 full prototype chip
  - Successor of SVX2 and SVX3 chip
  - DØ and CDF use the same chip
  - 0.25 μm technology, intrinsically rad-hard
  - DØ operates the chip in DØ-mode (dead-time)
- SVX4 chip works !!
  - Major success and gives both projects an excellent head start for full-scale testing of all elements of the detector
  - Chip testing at LBL and Fermilab
- Sample list of verifications done
  - ENC = 300e + 41e/pF C (Fermilab)
  - ENC = 600e + 32e/pF C (LBL)
- Known problems
  - Add pull-up to USESEU
  - Add pullup or pulldown to DØ-mode
  - Pull MSB of ChipID high.
  - Logic changes to FECLK gating/ADC control/FE control in DØ-mode



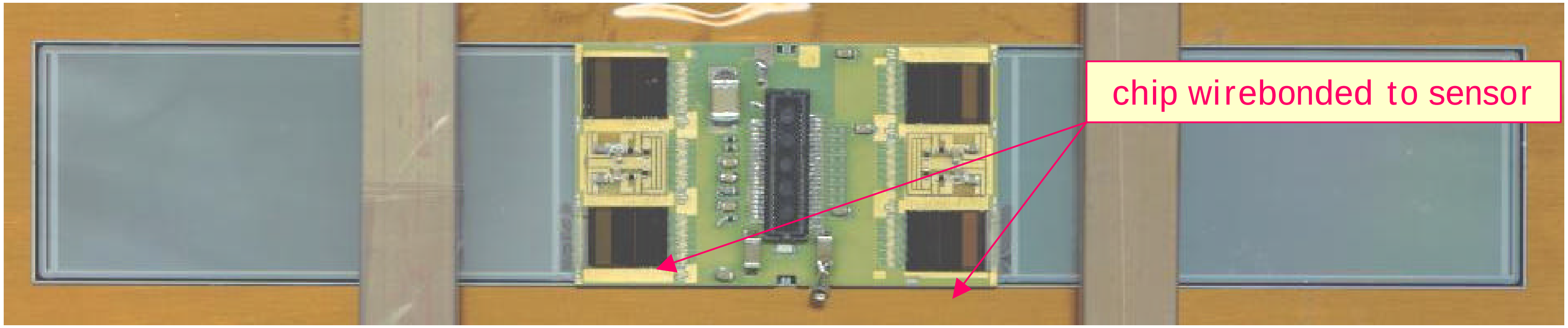
Hybrids

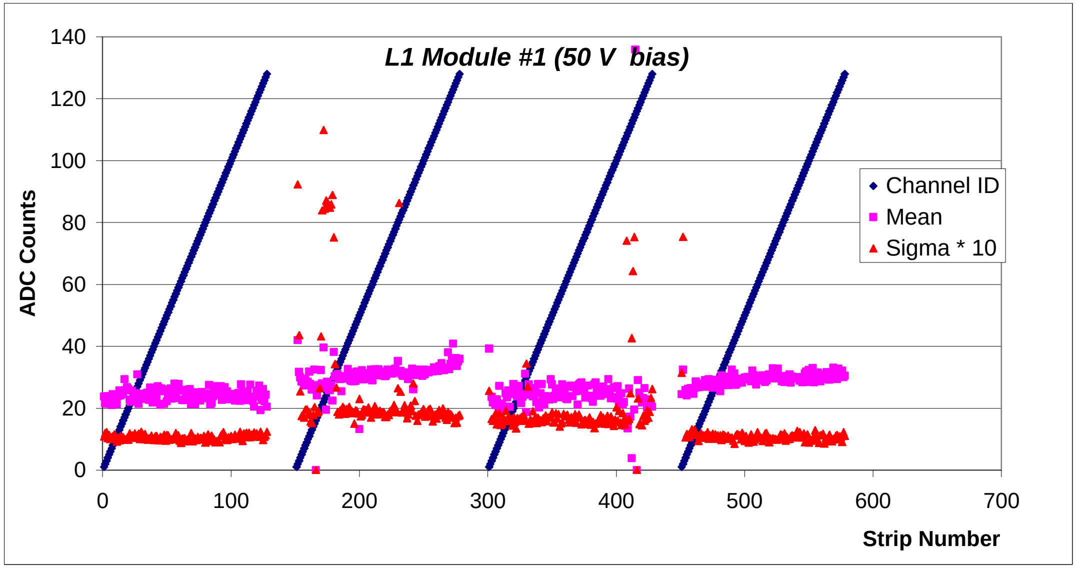
- **Design**
  - **BeO substrate with multi-layer circuit on substrate**
    - **6 Au layers and 5 dielectric layers**
    - **Use screen printing; min. via size 8 mils, ~10 mil spacing**
  - **Four types of hybrids**
    - **Layer 0: two-chip**
    - **Layer 1: six-chips, double-ended**
    - **Layer 2-5: ten-chips, double-ended**
      - **axial and stereo (only different in width)**
  - **Use 50 pin AVX 5046 connector**
- **Prototypes**
  - **Prototypes received from 2 vendors**
  - **Stuffed w/untested prototype SVX4 chips**
    - **Able to readout on first attempt!**
  - **In the process of qualifying both vendors**

L2-5 axial Hybrid



Layer 1 Readout Module





- Detector biased to 50V
- Noise slightly higher for chip 2 and 3
- Sigma of pedestal
  ~ 1 ADC count (no sensor)
  ~ 1.8 ADC counts w/ sensor
  Meets spec.
- Proof of principle that SVX4 + Hybrid + Readout System work !
- Chip 2 and 3 wirebonded to sensor
- Tests continue

Summary of Prototyping

Component	Vendor	Design	First Prototype Ordered	First Prototype Delivered	Second Prototype Ordered	Second Prototype Delivered
L0 Sensors	ELMA	✓	✓	✓		
	HPK	✓				
L1 Sensors	ELMA	✓	✓	✓		
	HPK	✓	✓	✓		
L2 Sensors		✓	✓			
Analogue Cable	Dycx	✓	✓	✓	✓	✓
L0 Hybrid		✓				
L1 Hybrid	CPT	✓	✓	✓		
L2A Hybrid	CPT	✓	✓			
	Amitr.	✓	✓	✓		
L2S Hybrid	CPT	✓	✓			
Digital Cable	Honey	✓	✓	✓	✓	✓
	Basic	✓	✓	✓	✓	
Junction Card		✓	✓	✓		
Twisted Pr. Cable		✓	✓	✓		
Adapter Card		✓	✓	✓		
Purple Card		✓	✓	✓	✓	
Test Stand Elctr.		✓	✓	✓		

- **Except for Layer 0 hybrids, have prototypes of all components in hand and no major issues have been encountered so far**

Summary and Conclusions

- Potential for Higgs observation at Fermilab with 15 fb^{-1}
- Radiation damage forces a new silicon tracker at 2-4 fb^{-1}
- Improved b-tagging with smaller inner radius
- Higher rates require better pattern recognition; more layers and larger outer radius
- Silicon must be built quickly to capitalize on opportunity for discovery
- A robust, straight-forward design has been developed and prototyping is well underway
- Already have first fully functional prototype module
- Lehman Review comment "Never before was a project baselined in such a state of technical maturity"
- Final funding awaits Tevatron review underway currently